SGS-THOMSON MICROELECTRONICS

QUALITY & RELIABILITY REPORT

April 1995 to March 1996 - EPROM, FLASH Memory, EEPROM and SRAM Products

INTRODUCTION

SGS-THOMSON manufactures a wide range of memory types which include:

Non-volatile memories: FLASH Memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; FLASH Memories in 1.2 to 0.6µ CMOS technology; OTP EPROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Static RAMs: Fast SRAM, both Synchronous and Asynchronous and NVRAMs (ZEROPOWER and TIMEKEEPER ranges). Fast SRAMs are manufactured in 0.7-0.6µ HCMOS technology; NVRAMs in 1.2-0.8µ HCMOS.

Packages for Static RAM products include the plastic PDIP, PLCC and SOJ. Some of the ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from April 1995 to March 1996. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

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Table 1. Final Average Outgoing Quality (AOQ), April 1995 to March 1996

Process	Electrical ppm				Visual ppm			
	4Q95	1Q96			4Q95	1Q96		
UV EPROM								
CMOS	14	19			24	15		
NMOS	0	0			14	0		
OTP EPROM								
CMOS	20	8			8	14		
FLASH								
CMOS	14	7			5	13		
SRAM								
CMOS	14	7			3	3		
EEPROM								
CMOS	0	1			10	12		

Table 2. Failure Rate Predictions, April 1995 to March 1996

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -20%	3.85	140	0.6	4.0	1,057	0	0.8	2.2
CMOS E5 -35%	5.27	140	0.6	4.0	1,446	0	0.6	1.6
NMOS E3	5.00	140	0.6	2.6	647	0	1.4	3.5
OTP EPROM								
CMOS E5 -20%	2.41	140	0.6	4.0	624	0	1.4	3.7
CMOS E5 -35%	1.42	140	0.6	4.0	367	0	2.5	6.3
FLASH								
CMOS T4	2.33	140	0.6	3.0	453	0	2.0	5.0
CMOS T5	4.05	140	0.6	4.0	1,051	0	0.9	2.2
CMOS T5 -20%	8.39	140	0.6	4.0	2,174	0	0.4	1.0
CMOS T6	2.98	140	0.6	4.6	889	0	1.0	2.6
SRAM								
CMOS Spectrum	0.33	125	0.7	64	1,635	0	0.6	1.4
HCMOS S3	0.51	125	0.7	64	2,513	2	1.2	2.1
HCMOS 4P	4.41	125	0.7	5.7	1,936	6	3.8	5.4
HCMOS 4PS	2.93	125	0.7	13	2,869	8	3.3	4.5
HCMOS 4PL	1.83	125	0.7	58	8,190	1	0.2	0.5
EEPROM								
CMOS F4	2.91	140	0.6	3.0	682	0	1.3	3.4
CMOS F4S	1.61	140	0.6	3.0	378	0	2.4	6.1

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	237	0	204	0	14,301	0	7,547	0	6,746	0	3,228	0
		– 168 hrs	237	0	204	0	2,075	0	1,111	0	522	0	1,644	0
		– 500 hrs	237	0	204	0	1,272	0	234	0	522	0	846	0
		– 1000 hrs	237	0	204	0	1,272	0	234	0	522	0	846	0
Retention Bake	1008	250°C,												
		– 48 hrs	225	0	150	0	1,076	0	400	0	438	0	600	0
		– 168 hrs	225	0	150	0	1,076	0	400	0	438	0	600	0
		– 500 hrs	225	0	150	0	1,076	0	400	0	438	0	600	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	2,708	0
		– 168 hrs	321	0
		– 500 hrs	321	0
		– 1000 hrs	321	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	114	0
		– 168 hrs	114	0
		– 500 hrs	114	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 5. CMOS E5/0.8µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B (B) M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, (50% '0')		
		– 48 hrs	11,046	0
		– 168 hrs	175	0
		– 500 hrs	175	0
		– 1000 hrs	175	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C, (99% '0')		
		– 48 hrs	150	0
		– 168 hrs	150	0
		– 500 hrs	150	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 6. CMOS E5/0.8µm Process (-20% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512 (C)		M27C1001 (C)		M27C1024 (B)		M27C2001 (C)		M27C4002 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	14,705	0	747	0	2,173	0	458	0	8,050	0
		– 168 hrs	1,377	0	747	0	245	0	165	0	350	0
		– 500 hrs	1,377	0	747	0	245	0	165	0	175	0
		– 1000 hrs	1,377	0	747	0	245	0	165	0	175	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	1,038	0	246	0	175	0	50	0	176	0
		– 168 hrs	1,038	0	246	0	175	0	50	0	176	0
		– 500 hrs	900	0	246	0	175	0	50	0	176	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 7. CMOS E5/0.8µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)		M27C801		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	14,149	0	6,905	0	9,977	0	12,093	0	2,195	0
		– 168 hrs	2,907	0	268	0	3,586	0	308	0	347	0
		– 500 hrs	798	0	268	0	931	0	308	0	347	0
		– 1000 hrs	798	0	268	0	931	0	308	0	347	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	1,300	0	188	0	1,384	0	200	0	150	0
		– 168 hrs	1,300	0	188	0	1,384	0	200	0	150	0
		– 500 hrs	1,300	0	188	0	1,384	0	200	0	150	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,086 3,086 1,811	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,355	0
Resistance to Solvents	2015	4 Solvent Solutions	280	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	200	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9. CMOS E5/0.8µm Process (–10% Upgrade) OTP EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	792	0
		– 500 hrs	672	0
		– 1000 hrs	672	0
		– 2000 hrs	288	0
Retention Bake	1008	150°C,		
		– 168 hrs	878	0
		– 500 hrs	878	0
		– 1000 hrs	878	0
		– 2000 hrs	277	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 10. CMOS E5/0.8µm Process (–10% Upgrade) OTP EPROM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	650	0
		– 500 hrs	650	0
		– 1000 hrs	550	0
		– 2000 hrs	298	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	444	0
		– 96 hrs	444	0
		– 168 hrs	444	0
		– 240 hrs	139	0
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	780	0
		– 96 hrs	780	0
		– 168 hrs	780	0
		– 240 hrs	780	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	1,020	0
		– 500 cycles	1,020	0
		– 1000 cycles	1,020	0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	175	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	50	0
Resistance to Solvents	2015	4 Solvent Solutions	132	0

Table 11. CMOS E5/0.8µm Process (–20% Upgrade) OTP EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz												
		– 168 hrs	492	0	237	0	396	0	191	0	225	0	459	0
		– 500 hrs	432	0	237	0	396	0	191	0	225	0	432	0
		– 1000 hrs	432	0	237	0	396	0	191	0	225	0	432	0
		– 2000 hrs	144	0	48	0	96	0	-	-	-	-	192	0
Retention Bake	1008	150°C,												
		– 168 hrs	600	0	240	0	360	0	50	0	100	0	540	0
		– 500 hrs	600	0	240	0	360	0	50	0	100	0	540	0
		– 1000 hrs	600	0	240	0	360	0	50	0	100	0	540	0
		– 2000 hrs	120	0	-	-	180	0	-	-	-	-	290	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 12. CMOS E5/0.8µm Process (–20% Upgrade) OTP EPROM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	500	0	200	0	460	0	45	0	50	0	450	0
		– 500 hrs	500	0	200	0	460	0	45	0	50	0	450	0
		– 1000 hrs	400	0	200	0	460	0	45	0	50	0	450	0
		– 2000 hrs	100	0	50	0	160	0	-	-	-	-	200	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,												
		– 48 hrs	248	0	28	0	223	0	28	0	28	0	223	0
		– 96 hrs	248	0	28	0	223	0	28	0	28	0	223	0
		– 168 hrs	248	0	28	0	223	0	28	0	28	0	223	0
		– 240 hrs	55	0	-	-	84	0	-	-	-	0	56	0
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	580	0	120	0	420	0	50	0	75	0	476	0
		– 96 hrs	580	0	120	0	420	0	50	0	75	0	476	0
		– 168 hrs	580	0	120	0	420	0	50	0	75	0	476	0
		– 240 hrs	580	0	120	0	420	0	50	0	75	0	360	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	480	0	180	0	540	0	25	0	50	0	540	0
		– 500 cycles	480	0	180	0	540	0	25	0	50	0	540	0
		– 1000 cycles	480	0	180	0	480	0	25	0	50	0	540	0
Solderability:														
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 295/0											
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 50/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 256/0											

Table 13. CMOS E5/0.8µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz						
		– 168 hrs	384	0	418	0	471	0
		– 500 hrs	384	0	418	0	471	0
		– 1000 hrs	384	0	418	0	471	0
		– 2000 hrs	96	0	-	-	48	0
Retention Bake	1008	150°C,						
		– 168 hrs	450	0	190	0	600	0
		– 500 hrs	450	0	190	0	600	0
		– 1000 hrs	360	0	190	0	540	0
		– 2000 hrs	120	0	-	-	120	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 14. CMOS E5/0.8µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	300	0	245	0	300	0
		– 500 hrs	300	0	245	0	300	0
		– 1000 hrs	300	0	245	0	300	0
		– 2000 hrs	100	0	50	0	100	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	265	0	28	0	333	0
		– 96 hrs	265	0	28	0	333	0
		– 168 hrs	194	0	28	0	278	0
		– 240 hrs	56	0	28	0	56	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	420	0	220	0	480	0
		– 96 hrs	420	0	220	0	480	0
		– 168 hrs	420	0	220	0	480	0
		– 240 hrs	420	0	220	0	420	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	420	0	200	0	420	0
		– 500 cycles	420	0	200	0	420	0
		– 1000 cycles	360	0	200	0	360	0
Solderability:								
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 485/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 150/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 284/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T4/1.2µm Process FLASH Memory Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	21,913	0	31,597	0
		– 168 hrs	288	0	412	0
		– 500 hrs	288	0	412	0
		– 1000 hrs	288	0	412	0
		– 2000 hrs	192	0	172	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	298	0	705	0
		– 500 hrs	298	0	705	0
		– 1000 hrs	298	0	705	0
		– 2000 hrs	150	0	310	0
Write/Erase Cycling		1,000 cycles	3,188	0	6,464	0
		10,000 cycles	-	-	614	1 (a)
Retention Bake	1008	150°C, 36 hrs	3,188	0	6,464	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Erasing Failure, single bit failures.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 16. CMOS T4/1.2µm Process FLASH Memory Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	500	0	360	0
		– 500 hrs	500	0	360	0
		– 1000 hrs	500	0	360	0
		– 2000 hrs	150	0	160	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	82	0	134	0
		– 96 hrs	82	0	134	0
		– 168 hrs	82	0	134	0
		– 240 hrs	28	0	25	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	280	0	300	0
		– 96 hrs	280	0	300	0
		– 168 hrs	280	0	300	0
		– 240 hrs	280	0	300	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	300	0	260	0
		– 500 cycles	300	0	260	0
		– 1000 cycles	300	0	260	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	-	-	25	0
		– 500 cycles	-	-	25	0
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 225/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 50/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 220/0			

Table 17. CMOS T5/0.8µm Process FLASH Memory Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	38,695	0	80,026	0
		– 168 hrs	528	0	204	0
		– 500 hrs	528	0	204	0
		– 1000 hrs	528	0	204	0
		– 2000 hrs	288	0	204	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	448	0	360	0
		– 500 hrs	448	0	360	0
		– 1000 hrs	448	0	260	0
		– 2000 hrs	250	0	150	0
Retention Bake	1008	250°C,				
		– 168 hrs	146	0	-	-
		– 500 hrs	146	0	-	-
		– 1000 hrs	146	0	-	-
		– 2000 hrs	146	0	-	-
Write/Erase Cycling		1,000 cycles	7,605	2 (a)	14,742	0
		10,000 cycles	472	2 (b)	81	0
Retention Bake	1008	150°C, 36 hrs	7,605	0	14,742	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.
Fail b. Erasing Failure, single bit failure.

Table 18. CMOS T5/0.8µm Process FLASH Memory Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	150	0	200	0
		– 500 hrs	150	0	200	0
		– 1000 hrs	150	0	150	0
		– 2000 hrs	100	0	150	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	111	0	137	0
		– 96 hrs	111	0	137	0
		– 168 hrs	111	0	137	0
		– 240 hrs	28	0	110	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	160	0	160	0
		– 96 hrs	160	0	160	0
		– 168 hrs	160	0	160	0
		– 240 hrs	160	0	160	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	240	0	120	0
		– 500 cycles	240	0	120	0
		– 1000 cycles	240	0	120	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	-	-	25	0
		– 500 cycles	-	-	25	0
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 495/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 248/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 236/0			

Table 19. CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 24 hrs	8,614	0	8,858	0	198,813	0	18,826	0
		– 168 hrs	114	0	246	0	1,479	0	76	0
		– 500 hrs	114	0	246	0	1,479	0	76	0
		– 1000 hrs	114	0	246	0	1,479	0	76	0
		– 2000 hrs	114	0	246	0	518	0	-	-
Retention Bake (1)	1008	150°C,								
		– 168 hrs	50	0	100	0	1,873	0	50	0
		– 500 hrs	50	0	100	0	1,873	0	50	0
		– 1000 hrs	50	0	100	0	1,437	0	50	0
		– 2000 hrs	50	0	100	0	813	0	50	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	1,541	0	-	-
		– 500 hrs	-	-	-	-	1,541	0	-	-
		– 1000 hrs	-	-	-	-	1,541	0	-	-
		– 2000 hrs	-	-	-	-	1,223	0	-	-
Write/Erase Cycling		1,000 cycles	2,769	0	2,474	0	51,887	5 (a)	5,301	0
		10,000 cycles	-	-	-	-	496	1 (b)	210	2 (b)
Retention Bake	1008	150°C, 36 hrs	2,769	0	2,474	0	51,887	0	5,301	0

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.
Fail b. Erasing Failure, single bit failure.

Table 20. CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	96	0	96	0	930	0	48	0
		– 500 hrs	96	0	96	0	930	0	48	0
		– 1000 hrs	96	0	96	0	770	0	48	0
		– 2000 hrs	96	0	96	0	370	0	48	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	88	0	132	0	525	0	44	0
		– 96 hrs	88	0	132	0	525	0	44	0
		– 168 hrs	88	0	132	0	525	0	44	0
		– 240 hrs	88	0	132	0	219	0	44	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	160	0	250	0	940	0	170	0
		– 96 hrs	160	0	250	0	940	0	170	0
		– 168 hrs	160	0	250	0	940	0	170	0
		– 240 hrs	160	0	250	0	740	0	170	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	136	0	153	0	880	0	50	0
		– 500 cycles	136	0	153	0	880	0	50	0
		– 1000 cycles	136	0	153	0	880	0	50	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	100	0	-	-
		– 500 cycles	-	-	-	-	75	0	-	-
Solderability:										
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 365/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 150/0							
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 228/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 21. CMOS T6/0.6µm Process FLASH Memory Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 - M28F410 - M28F420	
			Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 24 hrs	117,493	0
		– 168 hrs	168	0
		– 500 hrs	168	0
		– 1000 hrs	168	0
		– 2000 hrs	-	-
Retention Bake (1)	1008	150°C,		
		– 168 hrs	300	0
		– 500 hrs	300	0
		– 1000 hrs	300	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 168 hrs	150	0
		– 500 hrs	150	0
		– 1000 hrs	150	0
		– 2000 hrs	-	-
Write/Erase Cycling		1,000 cycles	14,442	0
		10,000 cycles	1,160	1 (a)
		100,000 cycles	160	0
Retention Bake	1008	150°C, 36 hrs	14,442	0

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.

Table 22. CMOS T6/0.6µm Process FLASH Memory Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 - M28F410 - M28F420	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	244	0
		– 500 hrs	244	0
		– 1000 hrs	244	0
		– 2000 hrs	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	108	0
		– 96 hrs	108	0
		– 168 hrs	108	0
		– 240 hrs	108	0
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	320	0
		– 96 hrs	320	0
		– 168 hrs	320	0
		– 240 hrs	320	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	120	0
		– 500 cycles	120	0
		– 1000 cycles	120	0
Thermal Shock	1011	–55 to 125°C,		
		– 100 cycles	25	0
		– 500 cycles	25	0
Solderability:				
– TSOP, SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	100	0
Resistance to Solvents	2015	4 Solvent Solutions	48	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 23A. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	250	0	10,500	0	1,250	0	-	-
		– 168 hrs	250	0	2,500	0	250	0	-	-
		– 500 hrs	250	0	2,500	0	250	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	50	0	1,200	0	150	0	100	0
		– 500 hrs	50	0	1,200	0	150	0	100	0
		– 1000 hrs	50	0	1,200	0	150	0	100	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	1,150	0	200	0	-	-
		1,000,000 cycles	-	-	1,150	0	200	0	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	1,150	0	200	0	-	-

Table 23B. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28C64C		ST93C06C ST93C46C		ST95010		ST95020	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	491	0	10,200	0	-	-	-	-
		– 168 hrs	491	0	1,200	0	-	-	-	-
		– 500 hrs	491	0	1,200	0	-	-	-	-
		– 1000 hrs	249	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	816	0	700	0	60	0	60	0
		– 500 hrs	816	0	700	0	60	0	60	0
		– 1000 hrs	816	0	700	0	60	0	60	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	400	0	1,200	0	-	-	-	-
		1,000,000 cycles	-	-	1,100	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	400	0	1,200	0	-	-	-	-

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 24. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164		M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	60	0	1,140	0	120	0	270	0	478	0	620	0
		– 500 hrs	60	0	1,140	0	120	0	270	0	478	0	620	0
		– 1000 hrs	60	0	1,140	0	120	0	270	0	478	0	620	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	100	0	1,609	0	100	0	850	0	667	0	600	0
		– 96 hrs	100	0	1,609	0	100	0	850	0	667	0	600	0
		– 168 hrs	100	0	1,609	0	100	0	850	0	667	0	600	0
		– 240 hrs	100	0	1,609	0	100	0	850	0	667	0	600	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	100	0	1,550	0	100	0	850	0	576	0	600	0
		– 200 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,												
		– 500 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Solderability:														
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 312/0											
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 336/0											
– PLCC Package			Cumulative Sample/Fail = 25/0											
– TSOP Package			Cumulative Sample/Fail = 25/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 128/0											
Resististance to Surface Mount:														
– SO Package			Cumulative Sample/Fail = 825/0											
– TSOP Package			Cumulative Sample/Fail = -/-											

Table 25. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24LC21		ST24C16		ST24E32	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,														
		– 168 hrs	3,650	0	890	0	100	0	224	0	72	0	80	0	208	0
		– 500 hrs	650	0	890	0	100	0	224	0	72	0	80	0	208	0
		– 1000 hrs	50	0	240	0	49	0	224	0	-	-	80	0	208	-
Retention Bake	1008	150°C,														
		– 168 hrs	200	0	440	0	50	0	-	-	117	0	60	0	202	0
		– 500 hrs	200	0	440	0	50	0	-	-	117	0	60	0	202	0
		– 1000 hrs	200	0	440	0	50	0	-	-	57	0	60	0	202	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	400	0	450	0	100	0	-	-	58	0	-	-	-	-
		1,000,000 cycles	350	0	450	0	100	0	-	-	58	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	400	0	450	0	100	0	-	-	58	0	-	-	-	-

Table 26. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24E32		M2201	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,										
		– 168 hrs	240	0	180	0	-	-	80	0	-	-
		– 500 hrs	240	0	180	0	-	-	80	0	-	-
		– 1000 hrs	240	0	180	0	-	-	80	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,										
		– 48 hrs	300	0	670	0	100	0	520	0	60	0
		– 96 hrs	300	0	670	0	100	0	520	0	60	0
		– 168 hrs	300	0	670	0	100	0	520	0	60	0
		– 240 hrs	300	0	670	0	100	0	520	0	60	0
Temperature Cycling	1010	–65 to 150°C,										
		– 100 cycles	300	0	550	0	110	0	300	0	-	-
		– 200 cycles	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,										
		– 500 cycles	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-
Solderability:												
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 96/0									
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 192/0									
– PLCC Package			Cumulative Sample/Fail = -/-									
– TSOP Package			Cumulative Sample/Fail = -/-									
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 196/0									
Resististance to Surface Mount:												
– SO Package			Cumulative Sample/Fail = 200/0									
– TSOP Package			Cumulative Sample/Fail = -/-									

Table 27. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f =1MHz		
		– 168 hrs	668	0
		– 500 hrs	264	0
		– 1000 hrs	264	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 28. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 539 345 237	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 468 388	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	60	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 29. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f =1KHz		
		– 168 hrs	844	2 (a)
		– 500 hrs	651	0
		– 1000 hrs	304	0

Notes: Fail a. Low V_{CC} Functional.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 30. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 335 335 179	 0 0 0
Temperature Cycling SOIC	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 75 75 75 75	 0 0 0 0
Temperature Cycling CAPHAT	1010	–40 to 125°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 366 194 143 143	 0 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs	 - -	 - -
Resistance to Solvents	2015	4 Solvent Solutions	24	0

Table 31. HCMOS 4P/0.7µm Process SRAM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz		
		– 168 hrs	4,958	3 (a)
		– 500 hrs	2,324	2 (a)
		– 1000 hrs	1,894	1 (a)
		– 2000 hrs	1,860	0

Note: Fail a. All failures are due to single bits and are suspected to be related to particles as shown from past failure analysis results of similar type failures.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 32. HCMOS 4P/0.7µm Process SRAM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 505 380 380	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 228 228	 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 516 436 436 436	 0 0 0 0
Resistance to Solvents	2015	4 Solvent Solutions	-	-

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 33. HCMOS 4PS/0.6µm Process SRAM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M624256 M628128		M628032	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz				
		– 168 hrs	2,527	3 (a)	255	1 (d)
		– 500 hrs	1,993	1 (b)	254	1 (e)
		– 1000 hrs	1,992	1 (c)	253	1 (d)
		– 2000 hrs	597	0	-	-

Notes: Multiple process improvements have been implemented to address polysilicon particle reduction, and have been verified to reduce defects. Rendundant column failures are due to XRL laser issue now corrected.
Fail a. 1 multiple column due to M1/M2 oxide particle.
1 single bit, no defect found.
1 improperly blown laser link.
Fail b. Single bit failure due to particle between poly 2 and poly 3.
Fail c. 1 improperly blown laser link.
Fail d. Single bit failure at 0°C.
Fail e. I_{CC3} failure at 70°C.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 34. HCMOS 4PS/0.6µm Process SRAM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256		M628032	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	45	0	50	0
		– 500 hrs	45	0	50	0
		– 1000 hrs	45	0	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	135	0	135	0
		– 192 hrs	135	0	135	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	232	0	153	0
		– 300 cycles	232	0	153	0
		– 600 cycles	232	0	153	0
		– 1000 cycles	232	0	153	0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-			

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 35. HCMOS 4PL/0.5µm 3.3V Process SRAM Reliability Data, Die Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M638032	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 4.2V, f =1MHz		
		– 168 hrs	1,834	1 (a)
		– 500 hrs	1,833	0
		– 1000 hrs	1,833	0
		– 1500 hrs	1,833	0

Notes: Fail a. Single bit failure at 48 hrs due to scratch causing Si damage in the gate.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 36. HCMOS 4PL/0.5µm 3.3V Process SRAM Reliability Data, Package Related Tests, April 1995 to March 1996

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M638032	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 3.3V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 271 271 271 171	 0 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 3.3V, – 96 hrs – 192 hrs	 142 142	 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 231 231 231 231	 0 0 0 0
Resistance to Solvents	2015	4 Solvent Solutions	-	-

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 37. Statistical Process Control: NMOS E3/1.5µm Process UV EPROM, Rousset - France Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Gate Oxide Thickness	1.34	1.29	1.25	1.04	2.38	2.22	1.41	1.22
Interpoly Oxide Thickness (1)	2.05	1.11	1.53	1.45	2.06	1.80	1.08	1.06
Field Oxide Thickness	1.78	1.59	1.68	1.52	2.48	2.46	1.84	1.82
Intermediate Dielectric Thickness	4.52	4.40	7.28	7.02	5.31	5.11	3.01	2.76
Final P-Vapox Thickness	6.06	4.90	3.99	3.76	4.30	4.23	4.61	4.15
Polysilicon I Thickness	2.82	2.77	1.43	1.39	1.97	1.71	2.19	2.10
Polysilicon II Thickness	2.47	2.36	1.89	1.82	2.30	2.12	2.53	2.42
Aluminium 1% Si Thickness (SP1)	2.31	2.18	2.09	1.97	2.95	2.74	2.45	2.35
Polysilicon II Critical Dimensions	1.88	1.55	2.20	1.80	2.21	1.91	1.53	1.45
Active Area Critical Dimensions	3.67	3.13	1.44	1.36	3.18	3.13	2.61	2.15

Note: 1. To redefine the way to proceed, in the case of restart of recipe on a furnace.

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT Henancement 25 x 25 µm	2.17	2.13	2.98	2.78	2.46	2.46	2.28	2.27
VT Array 25 x 25 µm	2.85	2.45	4.50	4.06	4.25	3.75	2.96	2.69
VT Field	7.83	3.77	11.80	5.12	5.13	2.52	8.65	3.62
I_{DON} Depletion 25 x 25 µm	2.35	2.12	2.94	2.71	3.13	2.77	2.51	1.79
Polysilicon II Sheet Resistance	13.30	3.58	13.30	3.47	13.50	3.55	12.60	3.29
Buried Contact Chain Resistance	25.10	4.88	36.60	6.85	34.50	6.49	29.00	5.31
N+ Sheet Resistance	7.77	6.39	3.07	2.59	8.98	7.23	2.11	1.77
AL-Polysilicon II Contact Chain Resistance	9.91	4.55	12.80	5.74	10.80	5.07	10.50	4.84
AL-N+ Contact Chain Resistance	6.52	5.29	7.64	6.26	7.76	6.33	2.54	2.15

Table 38. Statistical Process Control: CMOS E5/0.8µm Process UV EPROM, Agrate - Italy R1 Diffusion Line

Key Process Parameters	1Q 95		2Q 95		4Q 95		1Q96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.23	2.22	3.17	3.10	2.48	2.46	2.47	2.46
Silicon Nitride Thickness	2.01	1.99	2.03	2.02	1.85	1.84	1.75	1.74
Field Oxide Thickness	1.41	1.40	1.85	1.81	1.72	1.72	1.95	1.92
Gate Oxide Thickness	2.01	1.95	2.34	2.24	2.04	2.01	1.67	1.60
Interpoly Oxide Thickness	1.90	1.82	1.67	1.56	1.47	1.35	2.51	2.46
Intermediate Dielectric Thickness	2.08	2.02	2.08	1.99	6.26	6.19	4.58	2.83
Polysilicon I Thickness	1.72	1.64	2.17	2.14	1.45	1.38	1.37	1.33
Active Area Critical Dimensions	1.94	1.69	3.24	3.15	2.34	2.33	2.19	1.99
Policide Critical Dimensions	1.53	1.41	2.46	2.27	2.00	1.94	2.05	1.95

Key Electrical Parameters	1Q 95		2Q 95		4Q 95		1Q96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.55	2.19	2.53	2.38	2.92	2.55	2.89	2.51
VT P-Channel 25 x 25 µm	2.58	2.14	2.00	1.54	2.33	1.84	1.92	1.54
VT Natural 25 x 25 µm	4.25	3.91	4.37	4.21	4.10	4.09	3.21	3.19
VT Memory Cell 0.8 x 0.8 µm	1.66	1.64	1.72	1.70	1.81	1.79	1.48	1.45
I_{DON} N-Channel 25 x 0.8 µm	3.10	2.98	3.12	2.90	4.44	4.26	3.67	3.51
N+ Active Area Contact Chain	5.73	4.46	7.07	5.39	2.11	2.03	7.65	6.10
AL-Tungsten Silicide Contact Chain Resistance	2.04	1.77	3.01	2.47	2.60	1.81	2.12	1.64

Note: No UV EPROM wafer production in 3Q95.

Table 39. Statistical Process Control: CMOS E5/0.8µm Process UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	2Q 95		3Q 95		4Q 95		1Q96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.78	1.68	1.74	1.67	2.06	1.81	2.19	2.16
Silicon Nitride Thickness	1.47	1.41	1.48	1.46	1.74	1.74	1.71	1.71
Field Oxide Thickness	2.53	2.22	1.57	1.48	2.14	2.04	1.97	1.96
Gate Oxide Thickness	1.44	1.43	1.44	1.44	1.57	1.49	1.66	1.51
Interpoly Oxide Thickness	1.37	1.34	1.47	1.34	1.44	1.41	1.59	1.51
Intermediate Dielectric Thickness	1.75	1.68	1.91	1.83	1.76	1.69	1.66	1.58
Polysilicon I Thickness	2.63	2.58	2.91	2.90	2.58	2.55	3.03	2.93
Active Area Critical Dimensions	1.59	1.37	1.67	1.51	1.77	1.45	1.90	1.86
Policide Critical Dimensions	1.72	1.67	1.76	1.68	1.47	1.40	1.51	1.49

Key Electrical Parameters	2Q 95		3Q 95		4Q 95		1Q96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.96	2.41	2.06	1.84	2.94	2.14	2.51	1.76
VT P-Channel 25 x 25 µm	3.28	3.22	2.53	2.56	2.74	1.93	2.30	1.53
VT Natural 25 x 25 µm	2.75	2.67	2.93	2.65	2.80	2.50	2.51	1.76
VT Memory Cell 0.8 x 0.8 µm	1.32	1.30	1.30	1.28	1.37	1.31	1.38	1.30
I_{DON} N-Channel 25 x 0.8 µm	2.52	2.39	2.00	1.84	1.96	1.75	2.16	2.05
N+ Active Area Contact Chain	4.39	3.78	4.60	4.19	6.11	5.48	3.89	3.61
AL-W Silicide Contact Chain Resistance	1.56	1.47	3.34	2.75	3.53	3.49	3.51	3.40

Table 40. Statistical Process Control: CMOS T5/0.8µm Process FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.37	1.35	1.41	1.40	1.85	1.81	2.01	1.96
Polysilicon I Thickness	1.65	1.60	1.72	1.64	2.17	2.14	1.45	1.42
Gate Oxide Thickness	2.10	2.10	2.12	2.06	2.06	1.99	3.07	3.03
Tunnel Oxide Thickness	1.42	1.39	1.43	1.41	1.84	1.83	2.39	2.38
ONO Bottom Oxide Thickness	1.74	1.40	1.58	1.57	1.40	1.36	1.57	1.49
ONO Nitride Thickness	1.34	1.30	1.26	1.25	1.47	1.44	1.50	1.44
ONO Top Oxide Thickness	2.21	2.19	1.96	1.93	2.25	2.23	1.60	1.59
Active Area Critical Dimensions	1.83	1.40	1.44	1.42	1.65	1.59	2.39	2.31
Polysilicon II Critical Dimensions	1.62	1.39	1.18 (1)	0.87	1.35	1.29	2.07	1.89

Notes: No T5 FLASH Memory wafer production in 4Q95 and 1Q96.
1. Low CPK is due to change of dimensional target to improve the access time.

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.38	1.81	2.80	2.79	1.69	1.55	1.56	1.50
VT P-Channel 25 x 25 µm	2.27	2.01	1.89	1.77	1.15 (1)	1.04 (1)	1.46	1.43
BV N-Channel 25 x 1.2 µm	4.54	3.90	4.59	4.59	3.56	3.48	1.44	1.41
BV P-Channel 25 x 1.6 µm	2.86	2.61	5.70	5.64	2.96	2.87	1.68	1.54
VT Memory Cell 0.8 x 0.8 µm	1.88	1.71	2.10	2.04	1.91	1.83	1.56	1.51
I_{DON} N-Channel 25 x 1.2 µm	2.24	1.84	2.24	2.14	1.45	1.34	1.78	1.75
Al-N+ Contact Chain	4.59	4.15	2.89	2.80	3.78	3.64	4.30	4.25
Al-W Silicide Contact Chain Resistance	2.56	2.50	2.62	2.60	4.45	4.36	2.05	1.94

Note: 1. Some runs with high variability of this parameter on furnace 5. A specific analysis is running.

Table 41. Statistical Process Control: CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 95		4Q 95		1Q96			
	CP	CPK	CP	CPK	CP	CPK		
Field Oxide Thickness	2.01	1.96	1.74	1.72	1.95	1.92		
Polysilicon I Thickness	1.45	1.42	1.45	1.38	1.37	1.32		
Gate Oxide Thickness	3.07	3.03	2.00	1.96	1.80	1.72		
Tunnel Oxide Thickness	2.39	2.38	1.84	1.58	1.80	1.69		
ONO Bottom Oxide Thickness	1.57	1.49	2.16	2.04	1.49	1.47		
ONO Nitride Thickness	1.50	1.44	1.39	1.36	1.38	1.34		
ONO Top Oxide Thickness	1.60	1.59	1.53	1.50	1.76	1.72		
Active Area Critical Dimensions	1.83	1.65	1.55	1.48	1.45	1.44		
Polysilicon II Critical Dimensions	1.95	1.88	1.72	1.56	1.84	1.77		

Key Electrical Parameters	3Q 95		4Q 95		1Q96			
	CP	CPK	CP	CPK	CP	CPK		
VT N-Channel 25 x 25 µm	1.59	1.44	1.78	1.58	1.88	1.74		
VT P-Channel 25 x 25 µm	1.54	1.45	1.60	1.56	1.59	1.44		
BV N-Channel 25 x 0.8 µm	3.69	3.38	3.96	3.89	2.72	2.03		
BV P-Channel 25 x 0.9 µm	2.30	2.26	2.15	1.98	2.72	1.92		
VT Memory Cell 0.8 x 0.8 µm	1.65	1.61	1.70	1.62	1.55	1.53		
I_{DON} N-Channel 25 x 0.8 µm	1.92	1.88	2.45	2.36	2.04	1.82		
Al-N+ Contact Chain	3.88	3.81	2.80	2.77	4.93	3.20		
Al-W Silicide Contact Chain Resistance	2.55	2.51	1.70	1.60	2.76	2.50		

Table 42. Statistical Process Control: UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	1Q 95		2Q 95		3Q 95		4Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Shear Test (D.A.)	(*)	3.66	(*)	2.82	(*)	3.25	(*)	6.70
Bond Strength (W.B.)	(*)	2.59	(*)	2.51	(*)	2.55	(*)	2.54
SN Thickness (Tin Plate)	1.62	1.43	1.56	1.43	1.56	1.50	1.53	1.36

Note: *. One side limit only (CPL).